



11-10-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Docket: BUR920020113US1

Filing Date: 07/02/03
Application No.: 10/604230
Applicant: Conti et al.

Examiner: Unassigned
Group Art Unit: Unassigned
Confirmation No.: Unknown

Title: **APPLYING PARAMETRIC TEST PATTERNS FOR HIGH PIN COUNT ASICs ON LOW PIN COUNT TESTERS.**

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR 1.56, 1.97, 1.98

Honorable Commissioner of Patents and Trademarks
Washington, D. C. 20231

Sir:

Applicants submit herewith form PTO-1449, listing patents, publications, or other information of which they are aware which they believe may be material to patentability pursuant to 37 CFR 1.56(b), and in respect of which there may be a duty to disclose under 37 CFR 1.56(a), together with legible copies of the patents, publications, or other information listed.

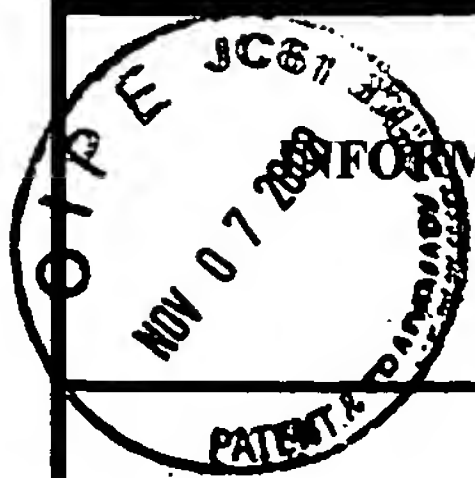
While the items submitted with this Information Disclosure Statement may be material to patentability pursuant to 37 CFR 1.56, in accordance with 37 CFR 1.97(h) it shall not be construed to be an admission that any patent, publication, or other information cited is "prior art" or is material to patentability for this invention unless specifically designated as such. In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other information material to patentability, as defined in 37 CFR 1.56(b), exists.

This Information Disclosure Statement is being filed with the filing of this application. Accordingly, it is not believed that any fee is required relating to the filing of this Information Disclosure Statement. If this is not the case, the Patent Office is hereby authorized to charge any related fee to Deposit Account No. 09-0456.

Respectfully submitted,

Date: 11/06/03

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INFORMATION DISCLOSURE CITATION
(Use several sheets if necessary)

Docket Number (Optional)

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Application Number

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Applicant(s)

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Group Art Unit

U.S. PATENT DOCUMENTS

| *EXAMINER INITIAL | REF | DOCUMENT NUMBER | DATE | NAME | CLASS | SUBCLASS | FILING DATE IF APPROPRIATE |
|----------------------|-----|-----------------|------|------|-------|----------|-------------------------------|
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FOREIGN PATENT DOCUMENTS

| | REF | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUBCLASS | Translation | |
|--|-----|-------------------|-------------------|-----------------------|-------|----------|-------------------------------------|----|
| | | | | | | | YES | NO |
| | | GB2342722A | 2000/04/19 | United Kingdom | | | <input checked="" type="checkbox"/> | |
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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

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|--|--|--|
| | | 'Special Test Chip For Testing IC Tester', IBM Technical Disclosure Bulletin, Vol. 28, No. 1, June 1985, pp. 221-222 |
| | | 'N-Way Testpoint For Complex LSI Design', IBM Technical Disclosure Bulletin, Vol. 13, No. 10, March 1972, pp. 2937-2938 |

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.